WHAT IS CLAIMED IS:

1. A system, comprising:

first circuitry in a first clock domain operable at a first clock frequency;

second circuitry in a second clock domain operable at a second clock frequency;

first and second jitter buffer pairs interfacing between said first circuitry and said second circuitry domain, said first jitter buffer pair comprising first and second jitter buffers, and said second jitter buffer pair comprising third and fourth jitter buffers;

wherein said first or second jitter buffers and said third or fourth jitter buffers alternately fill at said first clock frequency and empty at said second clock frequency, wherein alternation between said first and second jitter buffers and said third and fourth jitter buffers occurs at said second clocking frequency.

2. A system in accordance with claim 1, said first circuitry comprising an audio input, said second circuitry comprising an encoder.

3. A system in accordance with claim 1, said first circuitry comprising an audio output, said second circuitry comprising a decoder.

4. A system in accordance with claim 2, said first clock frequency comprising a sample clock, said second clock frequency comprising a frame clock.

5. A telecommunication system, comprising:

an audio input;

an audio output;

interface circuitry comprising first and second jitter buffers operably coupling said audio input to a voice encoder and third and fourth jitter buffers operably coupling said audio output to a voice decoder;

wherein said first or second jitter buffers alternately fill at a first clock frequency and empty at a second clock frequency, wherein alternation between said first and second jitter buffers occurs at said second clock frequency; and

wherein said third or fourth jitter buffers alternately fill at said second clock frequency and empty at said first clock frequency, wherein alternation between said third and fourth jitter buffers occurs at said second clock frequency.

6. A system in accordance with claim 5, said interface circuitry comprising one or more digital signal processors.

7. A system in accordance with claim 6, said first clocking frequency comprising a PCM sample clock frequency.

8. A system in accordance with claim 7, said second clock frequency comprising a frame clock frequency.

9. A system in accordance with claim 8, wherein a frame comprises 160 samples.

10. A system in accordance with claim 9, wherein a size of said first, second, third, and fourth buffers is 165 samples.

11. A method for rate adjustment using first and second jitter buffers, said first and second jitter buffers adapted to receive a plurality of samples at a first clock rate and transmit a block of said samples at a second clock rate, comprising:

switching between using said first or second jitter buffers at said second clock rate.

12. A method in accordance with claim 11, further including third and fourth jitter buffers, adapted to receive blocks of samples at said second clock rate and transmit a plurality of samples at said first clock rate, comprising:

switching between using said third or fourth jitter buffers at said second clock rate.

13. A method for rate adjustment, comprising:

receiving at first or second jitter buffers a plurality of samples at a first clock rate and transmit a block of said samples at a second clock rate; and

switching between using said first or second jitter buffers at said second clock rate.

14. A method in accordance with claim 13, further comprising:

receiving at third or fourth jitter buffers blocks of samples at said second clock rate and transmitting a plurality of samples at said first clock rate; and

switching between using said third or fourth jitter buffers at said second clock rate.

15. A method, comprising:

providing first circuitry in a first clock domain operable at a first clock frequency;

providing second circuitry in a second clock domain operable at a second clock frequency;

providing first and second jitter buffers interfacing between said first circuitry and said second circuitry domain;

wherein said first or second jitter buffers alternately fill at said first clock frequency and empty at said second clock frequency, wherein alternation between said first and second jitter buffers occurs at said second clocking frequency.

16. A method in accordance with claim 15, said first circuitry comprising an audio input, said second circuitry comprising an encoder.

17. A method in accordance with claim 15, said first circuitry comprising an audio output, said second circuitry comprising a decoder.

18. A method in accordance with claim 16, said first clock frequency comprising a sample clock, said second clock frequency comprising a frame clock.

19. A system, comprising:

first circuitry in a first clock domain operable at a first clock frequency;

second circuitry in a second clock domain operable at a second clock frequency;

first and second pairs of jitter buffers interfacing between said first circuitry and said second circuitry domain;

wherein ones of said pairs of first or second jitter buffers are swapped according to a clock by which said ones of said pairs of first or second jitter buffers are filled or emptied.

20. A system in accordance with claim 19, wherein said system is in a GSM/TDMA multi-mode phone.